IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of   :

Paul Rich   :   Group Art Unit: 1392

Application No. 10/760,464   :   Examiner: McDonald

Filed January 21, 2004   :

ELECTROSTATIC CLAMPING OF THIN WAFERS IN PLASMA PROCESSING VACUUM
CHAMBER

APPEAL BRIEF

U.S. Patent and Trademark Office
"eFILING"
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Sir:

     In connection with the above-identified application, please enter this Appeal Brief is in support of Applicant's appeal before the Board of Patent Appeals and Interferences.

TABLE OF CONTENTS

REAL PARTY IN INTEREST

The real party in interest is the assignee of record of the application, namely, Aviza Europe Limited, located Coed Rhedyn Ringland Way, Newport, Gwent, United Kingdom.

RELATED APPEALS AND INTERFERENCES

There are no prior or pending appeals, judicial proceedings or interferences known to the Appellant which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

STATUS OF CLAIMS

Claims 1-2 and 4-11 are pending in the application and all stand rejected. No claims are allowed.

Claims 1-2 and 4-11 are the claims appealed.

Claims 3 was cancelled.

STATUS OF AMENDMENTS

There have been no amendments to the appealed claims filed subsequent to final rejection.

SUMMARY OF CLAIMED SUBJECT MATTER

Thin wafer (250 microns or less) de-clamping during conventional plasma processing

As explained in the background section of the present application, thin wafers (250 microns or less, as defined in the specification at page 1, lines 22) exhibit relatively high bending or bowing forces during plasma processing. (Specification: page 2, lines 1-6.) Generally, electrostatic clamps are utilized to counter these forces and hence reduce wafer bowing. (Specification: page 2, lines 8-13.)

However, it has been found that thin wafers (250 microns or less) are especially prone to clamping failure which can lead to a complete detachment of the wafer from the electrostatic clamp during processing. (Specification: page 2, lines 13-15.) Applicants have determined that electrically conductive plasma present at the edge of the wafer can contribute to this clamping failure. In particular, the conductivity of the plasma can leak charge from the backside of the wafer, which in turn can disable the clamping force of the electrostatic clamp. (Specification: page 2, line 20, through page 3, line 5.)

The relevance of wafer thickness is presented by Applicants in the discussion relating to FIGS. 2 and 3 of the application.

That is, FIG. 2 illustrates backside pressurization gas flow over time at a power of about 12kW during sputter processing of a 380 microns thick wafer. No large increases in back side gas flow are observed, which means that no de-clamping (or de-chucking) of the wafer was evident. (Specification: page 7, lines 15-22.)

FIG. 3 illustrates backside pressurization gas flow over time at a power of about 12kW during sputter processing of a 100 microns thick wafer. In clear contrast to FIG. 2, it can be seen that significant back side gas flow has occurred and thus de-chucking has taken place. (Specification: page 7, lines 23-29.)

Apparatus Claims 1, 2, 4, 5, 6 and 9

Referring to the example of FIG. 4 of the drawings, the invention of independent **claim 1** is directed to an apparatus for processing a substrate 1 having a thickness of 250

microns or less (see discussion above). The apparatus includes a chamber (not shown), plasma creation element or elements (not shown) for creating a plasma 6 in a zone of the chamber, and an electrostatic chuck 2 for retaining a substrate 1 at a substrate location in or adjacent to the plasma 6 zone such that an upper surface of the substrate 1 faces away from the chuck 2. (Specification: page 6, lines 16, through page 7, line 6, referring to like elements of prior art FIG. 1.) The apparatus further includes a dark space 7 shield disposed on the plasma 6 zone side of the chuck 2 overlying a peripheral portion of the upper surface of the substrate 1 at a location for preventing the presence of plasma between the shield and the periphery portion of the upper surface of the substrate while allowing processing of the substrate. (Specification: page 8, lines 11-19.) A material forming the shield is an electrical conductor. (Specification: page 4, line 3.)

According to dependent **claim 2**, and as shown in FIG. 4, the shield 7 is generally annular and circumjacent the chuck 2. (Specification: page 3, line 21.)

According to dependent **claim 4**, the shield 7 is electrically grounded. (Specification: page 3, lines 3-4.)

According to dependent **claim 5**, the chuck 2 is a plasma creating element, and according to dependent **claim 6**, the chuck 2 is powered. (Specification: page 4, lines 5-6.)

According to dependent **claim 9**, the material forming the shield 7 is a metal. (Specification: page 9, lines 21.)

Method Claims 7, 8, 10 and 11

Referring by way of example to FIG. 4 of the drawings, the invention of independent **claim 7** is directed to processing a substrate 1 having thickness of 250 microns or less (see discussion above). The method includes electrostatically clamping the substrate 1 to a chuck 2, and creating a plasma 6 adjacent the outwardly facing face of the clamped substrate 1. (Specification: page 6, lines 16, through page 7, line 6,

referring to like elements of prior art FIG. 1.) The method further includes locating a dark space shield 7 overlying the periphery of the outwardly facing face of the clamped substrate 1 to prevent the presence of plasma 6 between the shield 7 and the periphery while allowing processing of the substrate 1. (Specification: page 8, lines 11-19.) The material forming the shield 7 is an electrical conductor. (Specification: page 4, line 3.)

According to dependent **claim 8**, the substrate thickness is less than or equal to 100 microns. (Specification: page 4, lines 15-16.)

According to dependent **claim 10**, the material forming the shield is a metal. (Specification: page 9, lines 21.)

According to dependent **claim 11**, the method further includes electrically grounding the shield. (Specification: page 3, lines 3-4.)

Thin wafer de-clamping avoid during plasma processing

Advantages achieved by Applicants invention are presented in the discussion relating to FIGS. 5 and 6 of the application.

That is, FIG. 5 illustrates backside pressurization gas flow over time in the case where a 98mm inner diameter dark space shield is positioned to surround the periphery of a 100mm diameter wafer. No large variations in back side gas flow are observed, which means that no de-clamping (or de-chucking) of the thin wafer was evident. (Specification: page 8, lines 20-28.)

For comparison, FIG. 6 illustrates backside pressurization gas flow in the case where the inner diameter of the dark space shield 7 is greater than the diameter of the wafer. Namely, the inner diameter of the shield 7 is 102mm and the diameter of the wafer is 100mm. As shown, the gas leakage increases significantly, but as explained in the specification, satisfactory performance may still be achieved for relatively short processing times. (Specification: page 8, line 29, through page 9, lines 11.)

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The grounds of rejection presented for review are as follows:

1.   The rejection of claims 1, 2, 7 and 8 under 35 U.S.C. §103 as being unpatentable over Mohn et al. (EP 0708478) in view of Francis (US 6465353).

2.   The rejection of claims 4-6 and 11 under 35 U.S.C. §103 as being unpatentable over Mohn et al. (EP 0708478) in view of Francis (US 6465353), and further in view of Weichart et al. (US 2003/0075522).

3.   The rejection of claims 9-11 under 35 U.S.C. §103 as being unpatentable over Mohn et al. (EP 0708478) in view of Francis (US 6465353), and further in view of Kravitz et al. (US 4426246) or Keyser et al. (US 4762728).

4.   The rejection of claims 1, 2, 4-6 and 11 under 35 U.S.C. §103 as being unpatentable over Weichart et al. (US 2003/0075522) in view of Francis (US 6465353) and Arnold et al. (US 5423971) or Scherer (GB 2310433) or Mohn et al. (EP 0708478).

5.   The rejection of claims 9 and 10 under 35 U.S.C. §103 as being unpatentable over Weichart et al. (US 2003/0075522) in view of Francis (US 6465353) and Arnold et al. (US 5423971) or Scherer (GB 2310433) or Mohn et al. (EP 0708478), and further in view of and further in view of Kravitz et al. (US 4426246) or Keyser et al. (US 4762728).

ARGUMENT

I. GENERAL OBSERVATIONS

Respectfully, the Examiner has not established a *prima facie* case of obviousness of the rejected claims.

In the rejections having Mohn et al. as the primary reference, the Examiner takes the position that silicon carbide (SiC) is an "electrical conductor", apparently because given the right conditions, SiC (like all materials) is *capable* of conducting electricity. Clearly, as discussed herein, one skilled in the art would not reasonably consider SiC an electric conductor. The Examiner takes the alternative position that even if SiC is not an electrical conductor, it would nevertheless be obvious to adopt such a configuration. Again, however, the Examiner's reasoning in this respect falls far short of establishing a *prima facie* case of obviousness. Moreover, the Examiner's assertions regarding grounding of the dark space shield as recited in dependent claims are clearly unsupported in the record.

In the rejections having Weichart et al. as the primary reference, the Examiner fails to appreciate the functional and positional differences between plasma excitation electrodes of Weichart et al. and the physical insulating plasma guard of Mohn et al. The Examiner appears to be modifying the references without regard to the reasons underlying the inclusion of the electrodes in Weichart et al.

II. WHETHER THE SUBJECT MATTER OF CLAIMS 1, 2, 7 AND 8 IS UNPATENTABLE UNDER 35 U.S.C. §103 OVER MOHN ET AL. (EP 0708478) IN VIEW OF FRANCIS (US 6465353)

Claims 1, 2, 7 and 8 stand rejected under 35 U.S.C. §103 as being unpatentable over Mohn et al. in view of Francis. Reversal of this rejection is requested.

In the rejection of record, the Examiner states:

> "... *Mohn et al. teach ... a shield 26 disposed on the zone*
> *side of the chuck overlying the peripheral portion of the*

*upper surface of the substrate 34 ... **Mohn et al. teach the***

shield can be electrically conducting since it can be made

of SiC. .(Column 3, lines 53)" *(Emphasis added.)*

Appellants strongly disagree that Mohn et al. teaches or suggests a shield made of a material which is an electrical conductor.

As is well know in the art, silicon carbide (SiC) is a semiconductor material which exhibits insulating properties in the absence of an applied voltage exceeding a threshold voltage. SiC is not an electrical conductor as the Examiner contends, nor are the remaining material examples listed at column 3, lines 53-54, of Mohn et al. Indeed, these materials are well known to function as insulators and/or insulating semiconductors.

The semi-conductive properties of SiC are notoriously well known in the art. As evidence thereof, attached is an article entitled "Influence of Microstructural Variation on the Electrical Properties of SiC Microthermistors." See, for example, the introduction section of this article.

The Examiner apparently contends that since SiC (like virtually all materials) can be made conductive if a high enough voltage is applied thereto, SiC constitutes a material which is "electrical conductor" as recited in the present claims. However, such contention is clearly not a reasonable interpretation of the phrase "electrical conductor". Moreover, Mohn et al. describes no conditions in which the SiC shield thereof would become conductive.

That is, Mohn et al. is devoid of any suggestion that the plasma guard 26 thereof could be, or should be, electrically conductive. For example, Mohn et al. makes no mention of applying a potential to the plasma guard 26 or grounding the plasma guard 26. Also, Mohn et al. attributes no electrically conductive function to the plasma guard 26 thereof.

Thus, it is clear that plasma guard 26 is in fact an insulating plasma guard.

The Examiner relies on Francis with respect to the claimed thickness of the wafer being processed. Indeed, Appellants have acknowledged the existence of such wafers in

the background section of the present specification. It is noted, however, that neither Mohn et al. nor Francis describe that thin wafers (250 microns or less) are especially prone to clamping failure which can lead to a complete detachment of the wafers from the electrostatic clamp during processing.

In any event, Mohn et al., taken alone or in combination with Francis, does not teach or suggest the provision of a dark space shield made of a material which is an electrical conductor, and for <u>at least</u> this reason, Appellants respectfully contend that claims 1, 2, 7 and 8 would not have been obvious to one of ordinary skill at the time the present invention was made.

III.   WHETHER THE SUBJECT MATTER OF CLAIMS 4-6 AND 11 IS UNPATENTABLE UNDER 35 U.S.C. §103 OVER MOHN ET AL. (EP 0708478) IN VIEW OF FRANCIS (US 6465353), AND FURTHER IN VIEW OF WEICHART ET AL. (US 2003/0075522)

Claims 4-6 and 11 stand rejected under 35 U.S.C. §103 as being unpatentable over Mohn et al. in view of Francis, and further in view of Weichart et al. Reversal of this rejection is requested.

<u>Claims 4 and 11</u>

The Examiner essentially takes the position that it would be obvious to ground the plasma guard of Mohn et al. in view of the teachings of Weichart et al.

However, as discussed above, the plasma guard of Mohn et al. is formed of a material which functions as an electrical insulator. It clearly would not be obvious to one of ordinary skill to ground the ring guard insulator of Mohn et al.

Further, in Weichart et al., element 5b referenced by the Examiner is counter-electrode that surrounds substrate table 8. See para. [0041] of Weichart. The counter-electrode 5b and another electrode 5a (which may be the table 8) function to "capacitatively excite" plasma within the chamber. With a high-frequency voltage applied to the electrode 5a (table 8), and the counter-electrode 5b grounded, the counter-electrode 5b is described as achieving dark space screening. See para. [0043] of Weichart.

The plasma guard of Mohn et al. is a physical barrier to plasma. In contrast, the counter-electrode 5b is an electrical element utilized to excite plasma. Further, the plasma guard of Mohn et al. and the counter-electrode 5b of Weichart et al. have entirely different orientations within the respective apparatus. Clearly, one skilled in the art would not be led to ground the plasma guard of Mohn et al. simply because Weichart et al. discloses a grounded excitation electrode surrounding a substrate table.

Thus, for at least the reasons stated above, and the reasons stated previously (Section II herein) with respect to independent claims 1 and 7, Appellants respectfully contend that claims 4 and 11 would not have been obvious to one of ordinary skill at the time the invention was made.

Claims 5 and 6

For at least the reasons stated previously (Section II herein) with respect to independent claim 1, Appellants respectfully contend that claims 5 and 6 would not have been obvious to one of ordinary skill at the time the invention was made.

IV.   WHETHER THE SUBJECT MATTER OF CLAIMS 9-11 IS UNPATENTABLE UNDER 35 U.S.C. §103 OVER MOHN ET AL. (EP 0708478) IN VIEW OF FRANCIS (US 6465353), AND FURTHER IN VIEW OF KRAVITZ ET AL. (US 4426246) OR KEYSER ET AL. (US 4762728)

Claims 9-11 stand rejected under 35 U.S.C. §103 as being unpatentable over Mohn et al. in view of Francis, and further in view of Kravitz et al. or Keyser et al. Reversal of this rejection is requested.

Dependent claims 9 and 10 recite the dark space shield as being formed of a metal. Dependent claim 11 recites the dark space shield as being grounded.

The Examiner relies on Kravitz et al. and Keyser et al. as allegedly teaching dark space shields made of metal which is grounded.

Again, however, Appellants respectfully point out that the plasma guard of Mohn et al. is a physical insulating barrier against plasma positioned over the upper periphery of the wafer.

In clear contrast, the dark space shield 32 of Keyser et al. is positioned around the cathode electrode 12 to inhibit the sputtering of oxygen containing materials from the gate insulating ring 14. See FIG. 1, and col. 4, lines 23-30, of Keyser et al.

Similarly, Kravitz et al. teaches a dark-space shield with an entirely different location and function than that of the plasma guard of Mohn et al. That is, the dark-space shield of Kravitz et al. is positioned to surround an electrode 52, and serves together with a perforated screen 56 to prevent discharge from occurring at the sides and bottom of the electrode 52. See FIG. 5, and col. 6, lines 51-59, of Kravitz et al.

The functions ascribed to the shields of Keyser et al. and Kravitz et al. are clearly distinct from that of the plasma guard of Mohn et al. The positional locations of the shields of Keyser et al. and Kravitz et al. are clearly distinct from that of the plasma guard of Mohn et al.

One of ordinary skill in the art would not be led to form the plasma guard of Mohn et al. of a metal or which is grounded simply because Keyser et al. and Kravitz et al. describe entirely different types of shields made of grounded metal.

Thus, for at least the reasons stated above, and the reasons stated previously (Section II herein) with respect to independent claims 1 and 7, Appellants respectfully contend that claims 9-11 would not have been obvious to one of ordinary skill at the time the invention was made.

V.   WHETHER THE SUBJECT MATTER OF CLAIMS 1, 2, 4-6 AND 11 IS UNPATENTABLE UNDER 35 U.S.C. §103 OVER WEICHART ET AL. (US 2003/0075522) IN VIEW OF FRANCIS (US 6465353) AND ARNOLD ET AL. (US 5423971) OR SCHERER (GB 2310433) OR MOHN ET AL. (EP 0708478)

Claims 1, 2, 4-6 and 11 stand rejected under 35 U.S.C. §103 as being unpatentable Weichart et al. in view of Francis and Arnold et al. or Scherer or Mohn et al. Appellants respectfully request reversal of this rejection.

The Examiner acknowledges Weichart et al. does not teach a dark space shield overlying a peripheral portion of an upper surface of a substrate, but contends that it

would be obvious to modify Weichart et al. in this respect based on the teachings of Arnold et al., Scherer or Mohn et al. Applicants respectfully disagree.

Again, in Weichart et al., element 5b referenced by the Examiner is counter-electrode that surrounds substrate table 8. See para. [0041] of Weichart. The counter-electrode 5b and another electrode 5a (which may be the table 8) function to "capacitatively excite" plasma within the chamber. With a high-frequency voltage applied to the electrode 5a (table 8), and the counter-electrode 5b grounded, the counter-electrode 5b is described as achieving dark space screening. See para. [0043] of Weichart et al. The Examiner has not shown that repositioning the electrode 5b of Weichart et al. which achieve the results desired by Weichart et al.

The dark space shields of Arnold (reference numbers 9 and 19) are designed to prevent the development of parasitic plasmas on the <u>back sides</u> of the electrodes 5 or 8. Also, with respect to the elements which are designated 60 and 61 of Arnold, the workpiece is fed from left to right through the chamber and thus these elements have no particular relationship with the substrate, and clearly the edges of the substrate would be exposed to the plasma in the chamber. A person skilled in the art would not combine the fixed process location of Weichart et al with the moving substrate of Arnold.

The dark space shield 6 of Scherer protects the <u>side wall 5</u> of the target, as is clearly described. Again there are moving substrates, this time rotary, which pass under an opening in the diaphragm 14. Even if the diaphragm 13 was a dark space shield (and it is not described as such in this document), the substrates moving under the opening 14 in the diaphragm would not be protected, nor would their carriers, in the manner set out in the claim. A person skilled in the art would not combine Weichart et al. with Scherer in the fashion apparently suggested by the Examiner.

Finally, the physical and functional differences between Weichart et al. and Mohn et al. have already been detailed (see Section III herein). Mohn et al. is directed to an insulating ring guard. In contrast, the counter-electrode 5b of Wiechart et al. clearly must be electrically conductive and functions in an entirely different manner than the ring guard of Mohn et al. It would not be obvious to one of ordinary skill to modify

the electrode 5b structure of Wiechart based on the insulating ring guard of Mohn et al.

Thus, for at least the reasons stated above, Appellants respectfully contend that claims 1, 2, 4-6 and 11 would not have been obvious to one of ordinary skill at the time the invention was made.

VI.   WHETHER THE SUBJECT MATTER OF CLAIMS 9 AND 10 UNDER IS UNPATENTABLE UNDER 35 U.S.C. §103 OVER WEICHART ET AL. (US 2003/0075522) IN VIEW OF FRANCIS (US 6465353) AND ARNOLD ET AL. (US 5423971) OR SCHERER (GB 2310433) OR MOHN ET AL. (EP 0708478), AND FURTHER IN VIEW OF AND FURTHER IN VIEW OF KRAVITZ ET AL. (US 4426246) OR KEYSER ET AL. (US 4762728)

Claims 9 and 10 stand rejected under 35 U.S.C. §103 as being unpatentable over Weichart et al. in view of Francis and Arnold et al. or Scherer or Mohn et al., and further in view of and further in view of Kravitz et al. or Keyser et al. Applicants respectfully request reversal of this rejection.

Dependent claims 9 and 10 recite the dark space shield as being formed of a metal.

The Examiner agains relies on Kravitz et al. and Keyser et al. as allegedly teaching dark space shields made of metal which is grounded.

Again, however, Appellants respectfully point out that the plasma guard of Mohn et al. is a physical insulating barrier against plasma positioned over the upper periphery of the wafer.

In clearly contrast, the dark space shield 32 of Keyser et al. is position around the cathode electrode 12 to inhibit the sputtering of oxygen containing materials from the gate insulating ring 14. See FIG. 1, and col. 4, lines 23-30, of Keyser et al.

Similarly, Kravitz et al. teaches a dark-space shield with an entirely different location and function than the plasma guard of Mohn et al. (i.e., modified Weichart et al.) That is, the dark-space shield of Kravitz et al. is positioned to surround an electrode 52, and serves together with perforated screen 56 to prevent discharge from occurring

at the sides and bottom of the electrode 52. See FIG. 5, and col. 6, lines 51-59, of Kravitz et al.

The functions ascribed to the shields of Keyser et al. and Kravitz et al. are clearly distinct from that of the plasma guard of Mohn et al. The positional locations of the shields of Keyser et al. and Kravitz et al. are clearly distinct from that of the plasma guard of Mohn et al.

One of ordinary skill in the art would not be led to form the plasma guard of Mohn et al. of a metal or which is grounded simply because Keyser et al. and Kravitz et al. describe entirely different types of shields made of grounded metal.

Thus, for at least the reasons stated above, and the reasons stated previously (Section V herein) with respect to independent claims 1 and 7, Appellants respectfully contend that claims 9 and 10 would not have been obvious to one of ordinary skill at the time the invention was made.

VII. CONCLUSION

For at least the reasons given herein, Appellant respectfully contends that the Examiner has not established a prima facie case of obviousness, and that the appealed claims define over the teachings of the applied references.

Reversal of each of the rejections of record is respectfully requested.

Respectfully submitted,

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CLAIMS APPENDIX

1. Apparatus for processing a substrate having a thickness of 250 microns or less, said apparatus including a chamber, plasma creation element or elements for creating a plasma in a zone of the chamber and an electrostatic chuck for retaining a substrate at a substrate location in or adjacent to the zone such that an upper surface of the substrate faces away from the chuck, wherein the apparatus further includes a dark space shield disposed on the zone side of the chuck overlying a peripheral portion of the upper surface of the substrate at a location for preventing the presence of plasma between the shield and the periphery portion of the upper surface of the substrate whilst allowing processing of the substrate, wherein a material forming the shield is an electrical conductor.

2. Apparatus as claimed in Claim 1 wherein the shield is generally annular an circumjacent the chuck.

4. Apparatus as claimed in Claim 1, wherein the shield is grounded.

5. Apparatus as claimed in Claim 1 wherein the chuck is also a plasma creating element.

6. Apparatus as claimed in Claim 1 wherein the chuck is powered.

7. A method for processing a substrate having thickness of 250 microns or less, said method comprising electrostatically clamping the substrate to a chuck, creating a plasma adjacent the outwardly facing face of the clamped substrate and locating a dark space shield overlying the periphery of the outwardly facing face of the clamped substrate to prevent the presence of plasma between the shield and the periphery whilst allowing processing of the substrate, wherein a material forming the shield is an

electrical conductor.

8. A method as claimed in Claim 7 wherein the substrate thickness is less than or equal to 100 microns.

9. Apparatus as claimed in Claim 1, wherein the material forming the shield is a metal.

10. Apparatus as claimed in Claim 7, wherein the material forming the shield is a metal.

11. Apparatus as claimed in Claim 7, further comprising electrically grounding the shield.

EVIDENCE APPENDIX

1.　　"Influence of Microstructural Variation on the Electrical Properties of SiC Microthermistors", by Takashi Terashige et al., IEEE Transactions On Electron Devices, Vol. 46, No. 3, pages 555-560, March 1999.

RELATED PROCEEDINGS APPENDIX

[There are no related proceedings.]

Influence of Microstructural Variation on the Electrical Properties of SiC Microthermistors

Takashi Terashige and Kazuo Okano, *Member, IEEE*

Abstract—The effects of the microstructural nonuniformity on the variations in the electrical properties of SiC ceramic were estimated quantitatively through simulations in order to produce microthermistors with the material. In these simulations, the grain size, the trap concentration at the grain boundary and the doping level in the grain were considered as the various microstructural nonuniformities. The device size was also taken into account as a parameter. The boundary potential model and the energy band model were used to express the electrical characteristics of the grain boundaries in the simulations. It is pointed out that those nonuniform microstructures greatly influence the electrical conductivity and the sensitivity of the SiC ceramic microthermistor. These phenomena are explained by the percolation theory. The tolerance of microstructural variation in the production of the ceramic is also discussed. It is revealed that the percolation threshold has the possibility to be used as an index of the acceptable microstructural tolerances.

Index Terms—Ceramics, high-temperature thermistor, numerical simulation, quality assurance, silicon carbide, variation.

I. INTRODUCTION

SILICON CARBIDE (SiC) ceramic is a material which is stable at high temperatures, and has a low manufacturing cost. For this reason, SiC ceramic has been used as a fireproof structural material, and is now spot-lighted to be used as a material for micromachines like turbines or engines, for which materials with excellent thermal and mechanical characteristics are required [1]. Moreover, the ceramic has the characteristics of a polycrystalline semiconductor [2], [3], and as such is expected to be used as a material for electronic devices such as a high-temperature thermistor [3], [4] or as a thermal battery. In order to use those devices in the micromachines mentioned above, the size of the device must be small as well, or in order to improve the response time of the thermistor, device size reduction is required in order to reduce the heat capacity.

The electrical properties of a ceramic semiconductor depend on its microstructure, namely, grain size, trap concentration at the grain boundary, defects, and the doping level in the grain, which depends on the manufacturing conditions. The microstructure is generally nonuniform, which influences the nonuniformity of the electrical properties of a ceramic semiconductor.

The effects of the nonuniformity mentioned above are more evident in the small devices. For this reason, quantitative investigation on the relation between the manufacturing process, the microstructure and the electrical properties is required before the design and the production of SiC ceramic micro devices like thermistors.

We have been trying to investigate these effects through simulations and have previously clarified the influence of the nonuniformity of the trap concentration at the grain boundary and the nonuniformity of the doping level in the grain [4], [5]. We have not as yet reported, however, the results of the investigations including the effects of grain-size nonuniformity nor mentioned the allowance of the variation in the microstructure for the production of the thermistors.

In this study, the variations in the electrical properties were estimated through simulations in order to produce SiC ceramic microthermistors. In these simulations, grain size, the trap concentration at the grain boundary and of the doping level in the grain were considered as the microstructural nonuniformities. The device size was also taken into account as a parameter. It is pointed out that those nonuniform microstructures greatly influence the electrical properties of the SiC ceramic microthermistor, on the basis of the results of the simulations. The allowance of microstructural variation for the production will also be mentioned.

II. MODELS AND ALGORITHM

SiC ceramics are made up of SiC crystal grains and grain boundaries, as shown in Fig. 1(a), with each grain considered to be a single crystalline semiconductor. The grain boundary is the interface at which a grain comes into contact with another grain of different crystal orientation, and at which dangling bonds exist. Based on the results from related experiments [2], [3], we assumed that the conduction of the semiconductor is P-type, and that the current flows in the grains and across the grain boundaries, but does not flow along the grain boundaries.

Under these assumptions, the grain boundary has a positive charge, because the holes in each SiC grain are trapped by the dangling bonds in the grain boundary. As a result, negative space charges are distributed in the grain near the grain boundary because of ionized acceptors located there. The number of trapped holes in a grain boundary is expressed as $N_T S$, where N_T is the trap concentration in the grain boundary and S is the area of the grain boundary between two grains. The number of ionized acceptors in a grain is expressed as $N_A W S$, where N_A is the effective accepter concentration in
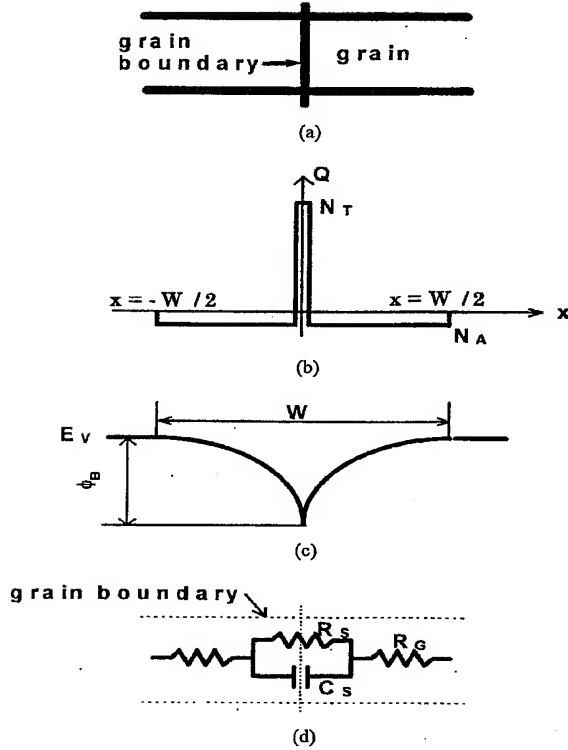
Fig. 1. Schematic models of the (a) microstructure, (b) charge distribution, (c) Schottky barrier, and (d) equivalent circuit.

the grain and W is the width of the space-charge layer. The number of holes, $N_T S$, is equal to the number of the accepters, $N_A W S$, because the trapped holes in the grain boundary come from the accepters in the grains on both sides, as shown in Fig. 1(b). Therefore the width of the space-charge layer is

$$W = \frac{N_T}{N_A}. \tag{1}$$

The barrier height Φ_B is calculated as follows. First, the electric field around the grain boundary is calculated based on the charge distribution. Using Poisson's equation

$$\frac{d^2 \Phi_B}{dx^2} = \frac{e \cdot N_A}{\varepsilon_0 \cdot \varepsilon_S} \ (0 < x \leqq W/2) \tag{2}$$

where ε_0 is the permittivity in vacuum and ε_S is the relative permittivity of SiC, for which the value of 10 is used here, considering the polytype of 3C or 6H. From the integration of (2), the barrier height Φ_B is obtained as

$$\Phi_B = \frac{e \cdot N_T^2}{8 \cdot \varepsilon_0 \cdot \varepsilon_S \cdot N_A}. \tag{3}$$

The equivalent circuit of a grain boundary is shown in Fig. 1(d). R_G is the resistance component in the grain, R_S is the resistance resulting from the Schottky barrier, and C_S is
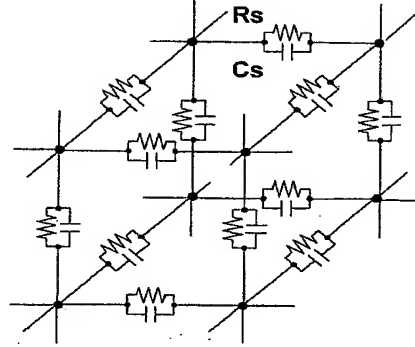

Fig. 2. Part of 3-D equivalent circuit used for simulations. Each pair of R_S and C_S corresponds to a grain boundary.

the capacitance around the grain boundary resulting from the space-charge layer. R_S is expressed as

$$R_S = R_0 \exp \left(\frac{e \cdot \Phi_B}{kT} \right) \tag{4}$$

where k is the Boltzmann constant, T is the temperature. R_0 is the resistance of R_S when T is infinite.

C_S is expressed as

$$C_S = \frac{\varepsilon_0 \varepsilon_S S}{W}. \tag{5}$$

The admittance of the Schottky barrier Y_S is given as

$$Y_S = \frac{1}{R_S} + j2\pi f C_S \tag{6}$$

where f is frequency.

As microstructural parameters, the variations of D, N_T, and N_A were taken into account. D is the size of a grain, N_T is the trap concentration in a grain boundary, and N_A is the accepter concentration in a grain. D was determined so that it has a normal distribution with a mean value of D_0 and a standard deviation of S_D. N_T and N_A were determined so that their logarithms have normal distributions with mean values of $\log N_{T0}$ and $\log N_{A0}$ and standard deviations of S_T and S_A, respectively. A random number generator was used in order to determine D, N_T, and N_A. Through the calculation procedure, pairs of R_S and C_S are obtained, from which Y_S can be determined using (6). These pairs of R_S and C_S are incorporated into the three-dimensional (3-D) circuit shown in Fig. 2. Each pair of R_S and C_S corresponds to a grain boundary. R_G in Fig. 1(d) is neglected because it is considered to be very small compared to R_S.

The size of the sample was assumed to be 30 μm in height (X) and 30 μm in width (Y) throughout these simulations as shown in Fig. 3. The length (Z) was varied from 30 to 100 μm as the device size parameter. The ohmic electrodes were assumed to be formed on the X–Y planes of the device ends. The grain size and the device size determine the number of the grain boundaries, i.e., the number of the pairs of R_S and C_S.
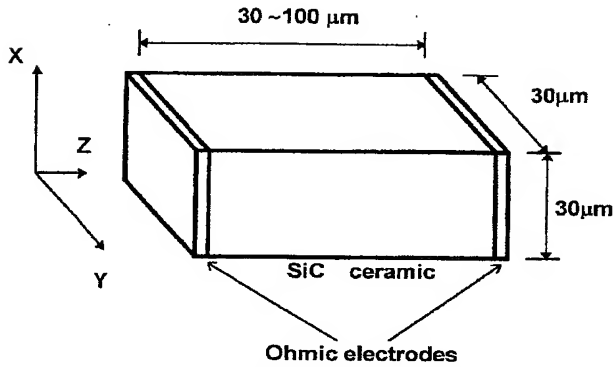
Fig. 3. Assumed device structure. The size is 30 μm in height (X) and 30 μm in width (Y). The length (Z) was varied from 30 to 100 μm as the device size parameter.

Then Kirchhoff's law is used in order to obtain the current, which is converted to the electrical conductivity (σ). The temperature dependence of σ is expressed as

$$\sigma = \sigma_0 \cdot \exp\left(-\frac{e \cdot \Phi_{BE}}{k \cdot T}\right) \qquad (7)$$

where Φ_{BE} is the effective barrier height which is obtained from the calculated results of σ, and σ_0 is the electrical conductivity when T is infinity. σ is also expressed as

$$\sigma = \sigma_1 \cdot \exp\left\{-B\left(\frac{1}{T} - \frac{1}{T_1}\right)\right\} \qquad (8)$$

where σ_1 is the electrical conductivity when T is T_1. B in (8) is called B constant, which indicates the sensitivity of a thermistor. The B constant is

$$B = \frac{e \cdot \Phi_{BE}}{k} \qquad (9)$$

from (7) and (8).

The flow of the simulation process is shown in Fig. 4. A random number generator was used in order to determine D, N_T, and N_A. Through a related experiment [2], [3], N_{T0}, N_{A0} were found to be about 8.8×10^{16} m^{-2} and 2.23×10^{25} m^{-3}. Also from related experiments, D_0 was found to be 4–8 μm. The frequency of the current is f and T is the temperature. A good agreement between the experimental results and the calculated results by this simulation method was obtained [4], which supports the validity of this simulation procedure.

III. RESULTS

Figs. 5 and 6 show the influences of the device size on the electrical properties of a SiC ceramic microthermistor for DC operation at 300 K. S_T was taken as a microstructural parameter and D_0 was assumed to be 5 μm with no variation ($S_D = 0$) for the calculations.

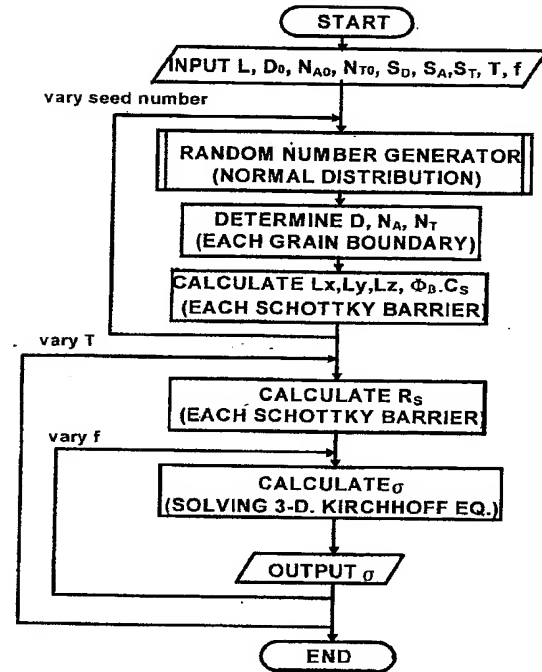Fig. 5 shows the effect of the device size on the average and the standard deviation of the electrical conductivity σ. The

Fig. 4. Flow chart for obtaining the electrical conductivity, σ, of the polycrystalline SiC ceramic semiconductor.
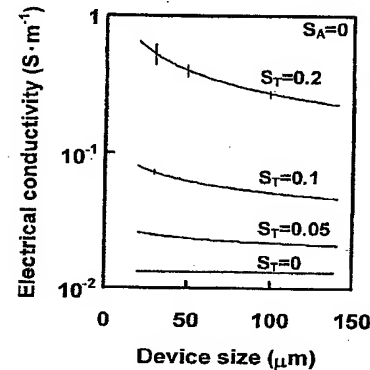

Fig. 5. Effects of the device size on the electrical conductivity σ. S_T is the standard deviation of logarithm of the trap concentration in a grain boundary. The curves are the average and the vertical bars across those lines indicate the widths of the variations, i.e., standard deviation of the electrical conductivity.

curves are the averages and the vertical bars across those lines indicate the widths of the variations, i.e., the averages plus or minus standard deviations at the cross points. As shown in Fig. 5, the reduction of the device size, i.e., the decrease of the number of the grain boundaries, tends to increase the average and the standard deviation. A larger S_T tends to increase the standard deviation of the electrical conductivity.

The influence of the size reduction on the B constant is shown in Fig. 6. The curves are the averages and the vertical bars across those lines indicate the widths of the variations as was done in Fig. 5. As shown in Fig. 6, the device size
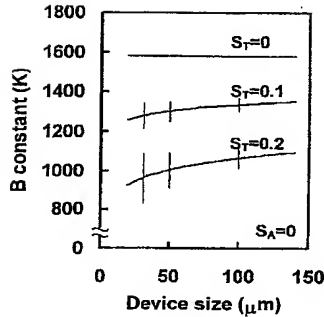
Fig. 6. Influence of the device size reduction on the B constant. The curves are the averages and the vertical bars across those lines indicate the widths of the variations.
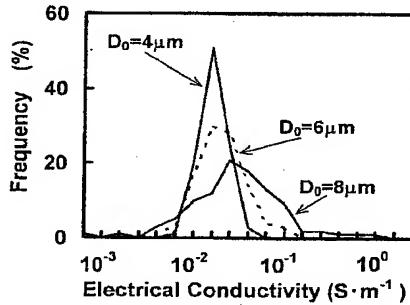

Fig. 7. Histogram of electrical conductivity, σ, when the average grain size D_0 is varied.

Fig. 8. Simplified model of R_S variation. R_H, R_A, and R_L stand for the resistors with high, average, and low resistance, respectively. Portions of (a) are shown in (b), (c), and (d). The bold vertical lines are electrodes.

reduction tends to increase the standard deviation of the B constant and to decrease the average.

The tendencies shown in Figs. 5 and 6 are drastic when the device size becomes below about 50 μm. Similar tendencies were obtained when S_A was used as the parameter [4]. The influence of S_T on σ is greater than that of S_A for the same device size because the influence of N_T is greater than that of N_A as shown by (3).

Fig. 7 is a histogram representing electrical conductivity when the average grain size D_0 is varied. In this calculation, the device length (Z in Fig. 3) was assumed to be 30 μm. A value of 0.3 was used for each of S_A and S_T. S_D was assumed to be 1.5 μm. The variation tended to widen and the average tended to increase with an increase in D_0 as shown in Fig. 7. The standard deviation drastically increases with increases in average grain size D_0.

IV. DISCUSSION

These results are related to the number of grain boundaries in a device and explained by the percolation theory [6]–[8] as follows. The variation of N_T or N_A causes the variation of R_S, as shown by (3) and (4). As a simplified model of the variation of R_S, we consider the circuit network shown in Fig. 8, where R_S is classified into three categories, R_H, R_A, and R_L. In Fig. 8, R_H, R_A, and R_L stand for the resistors with high, average, and low resistance, respectively. In Fig. 8(b)–(d), there are portions of (a), and the bold vertical lines are electrodes.
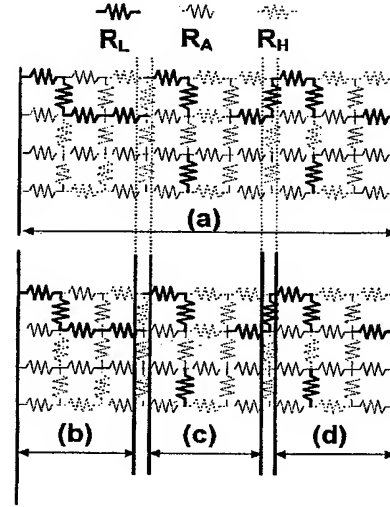
If the electrodes are linked only by the R_L's, the electrical conductivity σ increases because the current tends to flow only through paths that are made up only of the R_L's. The probability that the electrodes are connected only by the R_L's, which is called the percolation probability (P_C), depends on the number of resistors, i.e., the size of the circuit network as follows. In Fig. 8(a), the electrodes are not linked only by the R_L's. However in Fig. 8(b), the electrodes are linked only by the R_L's, though not linked in Fig. 8(c) and (d), for the same numbers of R_H's, R_A's, and R_L's. The electrical conductivity σ in Fig. 8(b) is higher than those of in Fig. 8(a)–(d) because there is a special path formed only by the R_L's and because there are no such special paths in Fig. 8(a), (c), and (d). This means that a device size reduction tends to increase the average, and the variation, of the electrical conductivity σ. The percolation probability also depends on the R_L-ratio which is defined as the ratio of number of the R_L's to the total number of resistors (R_S number).

For the further investigation of the relations between the percolation probability and the number of the resistors, several calculations were performed. The number of the resistors is assumed to be $5 \times 5 \times L$, related to the assumption noted in Section II. L is the number of the resistors between the electrodes along the Z direction. The calculated results are shown in Fig. 9. The ratio of R_L and R_H were assumed to be the same as shown in the inset in Fig. 9.

As shown in Fig. 9, the probability depends on L and on R_L-ratio. It is found from Fig. 9 that the decrease of L tends to make the percolation probability large for the same R_L-ratio, which is related to the difference between Fig. 8(a)–(d). The R_L-ratio at which the percolation probability begins to rise from 0%, which is called the percolation threshold, decreases with the decrease of L. This means that the influence of R_S variation on σ tends to occur even at small R_L-ratios and the influence becomes greater with the decrease of L.
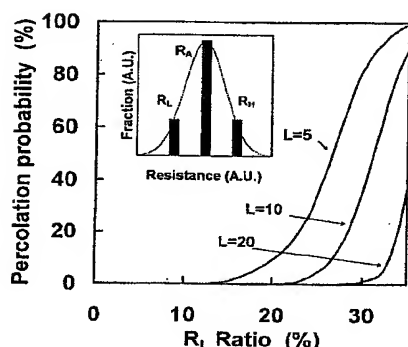
Fig. 9. Calculated results of the percolation probability. The inset shows the R_S variation. The ratio of R_L and R_H were assumed to be same.
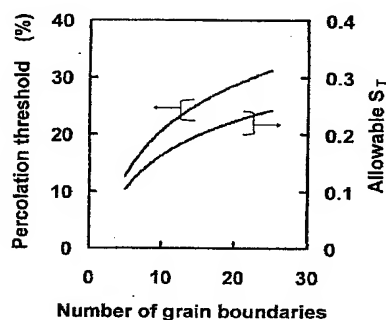

Fig. 10. Percolation threshold and the allowable S_T as functions of the number of grain boundaries. The allowable S_T was defined so that the ratio of the variation in the B constant to the average is within 5% when there is no variation but S_T.

Fig. 10 shows the percolation threshold and the allowable S_T as a function of the number of grain boundaries between electrodes along the Z direction (L). The allowable S_T was defined so that the ratio of the variation to the average of the B constant is within 5% when there is no variation but S_T. The allowable S_T and the percolation threshold have the same tendency as shown in Fig. 10. Thus the percolation probability is a good index of the influence of the R_S variation on σ. The percolation threshold has the potential to be used as a guideline for quality assurance in the manufacturing of these devices.

The actual situation is similar to the simplified cases mentioned above. The results shown in Figs. 5 and 7 are explained as follows. The N_T variation (S_T) and/or N_A variation (S_A) cause the variation of R_S, and some of the resistors have low resistance, which is related to the increase of the R_L-ratio mentioned above in Fig. 8. Then the percolation probability increases, and consequently makes the average and the variation of σ large. The influence is greater for the smaller sized devices or for the larger grain sizes, i.e., less grain boundaries, related to decrease of L in Fig. 9.

The results shown in Fig. 6 are also explained by the percolation theory. Each Φ_B is directly related to a respective R_S by (3) and the B constant is expressed by (9). The decrease of the B constant means that the effective height of the Schottky barrier (Φ_{BE}) decreases, as seen in (9), with the decrease of the grain boundaries. The N_T variation (S_T) and/or N_A variation (S_A) causes the variation of Φ_B and some Φ_B's have a low barrier height (low Φ_B). The current flows through the path, formed only by the low Φ_B, with a certain percolation probability. Then the formation of such a path tends to make the average of the B constant small and to make the variation wide as seen in (3) and (4). The influence of the Φ_B variation on the B constant becomes greater with the decrease of the number of grain boundaries as well as the influence on the σ.

Thus the results shown in Figs. 5–7 are explained by the percolation theory. The influence of the microstructural nonuniformity on the characteristics of a thermistor becomes greater with a device size reduction and/or a larger grain size. It is important to make the microstructure uniform and/or to make the grain size smaller, i.e., to increase the number of the grain boundaries in order to keep uniform characteristics for polycrystalline SiC. These parameters strongly depend on the process conditions, and we are currently conducting intensive efforts to determine these best conditions [3], [9].

V. CONCLUSIONS

The electrical properties of polycrystalline SiC ceramic were estimated through simulations in order to produce microthermistors from the material. From the results of these simulations, the following was revealed.

1) The variation in N_T or N_A causes the variations of Φ_B and R_S. Those variations also lead to the increase of the average σ, to the decrease of the average B constant, and to the increase of the variations in σ and the B constant.

2) Those variations are enhanced by the decrease in the number of grain boundaries between the electrodes resulting from a smaller device size or a larger D_0.

3) These phenomena mentioned above are explained by the percolation theory. The percolation threshold has the possibility to be used to indicate the acceptable tolerances of microstructural variations for the production of thermistors.

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